Kobayashi et al. also discloses in FIG. 14 another DLL for generating an internal clock signal (C") based a reference clock signal (C). In FIG. 14, Kobayashi et al. also discloses an internal circuit (500) which receives a delayed clock signal (C'). A selector (400) of Kobayashi et al. selects a signal at an output node of a delay line (303) to be the delayed clock signal during a normal operation. Selector 400 selects the reference clock signal C to be the delayed clock signal C' during a test. As shown in FIG. 14 of Kobayashi, regardless of which of the reference clock signal C and the signal at the output node of delay line 303 is selected to be the delayed clock signal C', the DLL of Kobayashi et al. performs a synchronization operation to synchronize the internal clock signal C" and the reference clock signal C.

With respect to independent claim 1, Applicant is unable to find, among other things, in Kobayashi et al. "a DLL controller having a selector connected to the DLL for selectively activating a DLL control signal during a test mode of the memory device to prevent the DLL from performing the synchronization operation during the test mode". Thus, claim 1 is not anticipated by Kobayashi et al. Therefore, Applicant requests that the rejection of claim 1 be reconsidered and withdrawn and that claim 1 and dependent claims of claim 1 be allowed.

With respect to independent claim 8, Applicant is unable to find, among other things, in Kobayashi et al. "a DLL controller having a selector connected to the DLL for selectively activating a DLL control signal during a test mode of the memory device to prevent the DLL from adjusting the delay during the test mode". Thus, claim 8 is not anticipated by Kobayashi et al. Therefore, Applicant requests that the rejection of claim 8 be reconsidered and withdrawn and that claim 8 and dependent claims of claim 8 be allowed.

With respect to independent claim 14, Applicant is unable to find, among other things, in Kobayashi et al. "a DLL controller having a selector connected to the DLL for selectively activating a DLL control signal to disable the shifting operation during the test mode". Thus, claim 14 is not anticipated by Kobayashi et al. Therefore, Applicant requests that the rejection of claim 14 be reconsidered and withdrawn and that claim 14 and dependent claims of claim 14 be allowed.

With respect to independent claim 19, Applicant is unable to find, among other things, in Kobayashi et al. "an output connected to the phase detector providing the DLL control signal for selectively disable the shifting operation based on the test select signal and the test control signal

during a test mode". Thus, claim 19 is not anticipated by Kobayashi et al. Therefore, Applicant requests that the rejection of claim 19 be reconsidered and withdrawn and that claim 19 and dependent claims of claim 19 be allowed.

With respect to independent claim 21, Applicant is unable to find, among other things, in Kobayashi et al. "a DLL controller having a selector connected to the DLL for selectively activating a DLL control signal during a test mode of the memory device to prevent the DLL from performing the synchronization operation during the test mode". Thus, claim 21 is not anticipated by Kobayashi et al. Therefore, Applicant requests that the rejection of claim 21 be reconsidered and withdrawn and that claim 21 and dependent claims of claim 21 be allowed.

With respect to independent claim 26, Applicant is unable to find, among other things, in Kobayashi et al. "a DLL controller having a selector connected to the DLL for selectively activating a DLL control signal during a test mode of the memory device to prevent the DLL from adjusting the delay during the test mode". Thus, claim 26 is not anticipated by Kobayashi et al. Therefore, Applicant requests that the rejection of claim 26 be reconsidered and withdrawn and that claim 26 and dependent claims of claim 26 be allowed.

With respect to independent claim 42, Applicant is unable to find, among other things, in Kobayashi et al. "a DLL controller having a selector connected to the DLL for generating a DLL control signal independently from the external clock signal during a test mode of the memory device to disable the synchronization operation for a suspension time during the test mode". Thus, claim 42 is not anticipated by Kobayashi et al. Therefore, Applicant requests that the rejection of claim 42 be reconsidered and withdrawn and that claim 42 and dependent claims of claim 42 be allowed.

With respect to independent claim 45, Applicant is unable to find, among other things, in Kobayashi et al. "a DLL controller having a selector connected to the DLL for activating a DLL control signal independently from the external clock signal during a test mode of the memory device to prevent the shift register from adjusting the delay during the test mode". Thus, claim 45 is not anticipated by Kobayashi et al. Therefore, Applicant requests that the rejection of claim 45 be reconsidered and withdrawn and that claim 45 and dependent claims of claim 45 be allowed.

With respect to independent claim 48, Applicant is unable to find, among other things, in Kobayashi et al. "a DLL controller having a selector connected to the DLL for activating a DLL control signal independently from the external clock signal to disable the shifting operation during the test mode". Thus, claim 48 is not anticipated by Kobayashi et al. Therefore, Applicant requests that the rejection of claim 48 be reconsidered and withdrawn and that claim 48 and dependent claims of claim 48 be allowed.

With respect to independent claim 51, Applicant is unable to find, among other things, in Kobayashi et al. "a DLL controller having a selector connected to the DLL for activating a DLL control signal independently from the external clock signal to disable the shifting operation during the test mode". Thus, claim 51 is not anticipated by Kobayashi et al. Therefore, Applicant requests that the rejection of claim 51 be reconsidered and withdrawn and that claim 51 and dependent claims of claim 51 be allowed.

Claims 1-29 and 42-53 were rejected under 35 USC § 102(e) as being anticipated by Lee et al. (U.S. Patent No. 6,486,651).

Applicant respectfully traverses.

Lee et al. discloses several DLL: DLL 200 in FIG. 1, DLL 4 and DLL 6 in FIG. 3. Lee et al. also discloses several selectors (circuit 204 in FIG. 1) and (selectors 40, 70, and 40' in FIG. 3). The selectors of Lee et al. select clock signals with different frequencies to test the DLL during a test. The selectors of Lee et al. do not activate a DLL control signal during the test to prevent a synchronization operation of the DLL.

With respect to independent claim 1, Applicant is unable to find, among other things, in Lee et al. "a DLL controller having a selector connected to the DLL for selectively activating a DLL control signal during a test mode of the memory device to prevent the DLL from performing the synchronization operation during the test mode". Thus, claim 1 is not anticipated by Lee et al. Therefore, Applicant requests that the rejection of claim 1 be reconsidered and withdrawn and that claim 1 and dependent claims of claim 1 be allowed.

With respect to independent claim 8, Applicant is unable to find, among other things, in Lee et al. "a DLL controller having a selector connected to the DLL for selectively activating a DLL control signal during a test mode of the memory device to prevent the DLL from adjusting the delay during the test mode". Thus, claim 8 is not anticipated by Lee et al. Therefore,

Applicant requests that the rejection of claim 8 be reconsidered and withdrawn and that claim 8 and dependent claims of claim 8 be allowed.

With respect to independent claim 14, Applicant is unable to find, among other things, in Lee et al. "a DLL controller having a selector connected to the DLL for selectively activating a DLL control signal to disable the shifting operation during the test mode". Thus, claim 14 is not anticipated by Lee et al. Therefore, Applicant requests that the rejection of claim 14 be reconsidered and withdrawn and that claim 14 and dependent claims of claim 14 be allowed.

With respect to independent claim 19, Applicant is unable to find, among other things, in Lee et al. "an output connected to the phase detector providing the DLL control signal for selectively disable the shifting operation based on the test select signal and the test control signal during a test mode". Thus, claim 19 is not anticipated by Lee et al. Therefore, Applicant requests that the rejection of claim 19 be reconsidered and withdrawn and that claim 19 and dependent claims of claim 19 be allowed.

With respect to independent claim 21, Applicant is unable to find, among other things, in Lee et al. "a DLL controller having a selector connected to the DLL for selectively activating a DLL control signal during a test mode of the memory device to prevent the DLL from performing the synchronization operation during the test mode". Thus, claim 21 is not anticipated by Lee et al. Therefore, Applicant requests that the rejection of claim 21 be reconsidered and withdrawn and that claim 21 and dependent claims of claim 21 be allowed.

With respect to independent claim 26, Applicant is unable to find, among other things, in Lee et al. "a DLL controller having a selector connected to the DLL for selectively activating a DLL control signal during a test mode of the memory device to prevent the DLL from adjusting the delay during the test mode". Thus, claim 26 is not anticipated by Lee et al. Therefore, Applicant requests that the rejection of claim 26 be reconsidered and withdrawn and that claim 26 and dependent claims of claim 26 be allowed.

With respect to independent claim 42, Applicant is unable to find, among other things, in Lee et al. "a DLL controller having a selector connected to the DLL for generating a DLL control signal independently from the external clock signal during a test mode of the memory device to disable the synchronization operation for a suspension time during the test mode". Thus, claim 42 is not anticipated by Lee et al. Therefore, Applicant requests that the rejection of

claim 42 be reconsidered and withdrawn and that claim 42 and dependent claims of claim 42 be allowed.

With respect to independent claim 45, Applicant is unable to find, among other things, in Lee et al. "a DLL controller having a selector connected to the DLL for activating a DLL control signal independently from the external clock signal during a test mode of the memory device to prevent the shift register from adjusting the delay during the test mode". Thus, claim 45 is not anticipated by Lee et al. Therefore, Applicant requests that the rejection of claim 45 be reconsidered and withdrawn and that claim 45 and dependent claims of claim 45 be allowed.

With respect to independent claim 48, Applicant is unable to find, among other things, in Lee et al. "a DLL controller having a selector connected to the DLL for activating a DLL control signal independently from the external clock signal to disable the shifting operation during the test mode". Thus, claim 48 is not anticipated by Lee et al. Therefore, Applicant requests that the rejection of claim 48 be reconsidered and withdrawn and that claim 48 and dependent claims of claim 48 be allowed.

With respect to independent claim 51, Applicant is unable to find, among other things, in Lee et al. "a DLL controller having a selector connected to the DLL for activating a DLL control signal independently from the external clock signal to disable the shifting operation during the test mode". Thus, claim 51 is not anticipated by Lee et al. Therefore, Applicant requests that the rejection of claim 51 be reconsidered and withdrawn and that claim 51 and dependent claims of claim 51 be allowed.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's representative at (612) 373-6969 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 29 day of April, 2004.

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